Remarks

Claims 1-10, 12, 13, 15, 16 and 18 stand rejected and are canceled herein. Claims 11, 14 and 17 were canceled in a previous response. New claims 19-34 are added herein, and thus remain pending. The Assignee respectfully traverses the rejection and requests allowance of claims 19-34.

Title Amendment

The title is amended herein to more closely align its language with the claimed subject matter of the present application.

Claim Amendments

Claims 1-10, 12, 13, 15, 16 and 18 are canceled herein, resulting in claims 1-18 inclusive being canceled.

New claims 19-34 have been added to address various logical and grammatical deficiencies in the previously pending claims. Support for the new claims may be found in the current application at Figs. 3-5, and at paragraphs [0013] through [0019]. Thus, no new matter has been added.

Claim Rejection Under 35 U.S.C. § 102

Claims 1-10, 12, 13, 15, 16 and 18 stand rejected under 35 U.S.C. § 102(e) as being anticipated by "Hyper-Threading Technology Architecture and Microarchitecture," *Intel Technology Journal*, vol. 06, no. 01 (hereinafter "Intel"). (Page 2 of the final Office action.) The Assignee respectfully traverses the rejection in light of new claims 19-34, and in view of the following discussion.

New independent method claim 19 provides for processing instructions in clusters of execution units according to either a throughput mode or a wide mode of operation. In throughput mode, bundles of instructions from a first execution thread of a program are distributed to a first cluster for processing, while bundles of instructions from a second thread are distributed to a second cluster, so that overall throughput of the two threads may be enhanced. In wide mode, instruction bundles of a third thread are distributed among both the first and second

clusters to facilitate faster processing of that third thread. New independent processor claim 31 provides similar limitations.

The Assignee traverses the rejection because Intel does not teach or suggest first and second clusters of execution units, and does not teach or suggest throughput and wide modes of operations, as provided for in claims 19 and 31. Each of these issues is discussed separately below.

First and Second Clusters of Execution Units

Generally, Intel discusses a processor architecture in which "a *single physical processor appear[s]* as multiple *logical* processors." (Page 6, right column, first paragraph of Hyper-Threading Technology Architecture; emphasis supplied.) In this architecture, "[t]here is one copy of the architecture state for each logical processor, and the logical processors *share a single set of physical execution resources.*" (Id.; emphasis supplied.) This single set of physical execution resources, or execution units, represents at most a *single* physical cluster or core. (Please see Fig. 4, which describes a single processor Xeon™ processor pipeline with a single out-of-order execution engine. Further, please see Fig. 6, which shows that the single engine includes *one* set of execution units. See also the "Execution Units" subsection in the left column of page 11, which refers to a single physical register file.) Please also note that the execution units are *not* partitioned between logical processors, as the execution units are "largely oblivious to logical processors." (See first paragraph of the "Execution Units" section.)

The final Office action appears to associate the *logical processors* of Xeon with the clusters of claims 19 and 31. (Page 13 of the final Office action, for example.) However, the Assignee respectfully contends that the logical processors, each of which are represented in Xeon only by way of architecture states within the processor, are not physical or actual processors, but instead share execution time on a single physical processor, core, or cluster, as only one such processor exists.

Thus, Intel does not teach or suggest the use of multiple clusters of execution units, as provided for in claims 19 and 31, and such indication is respectfully requested.

Throughput and Wide Modes of Operation

The final Office action also appears to rely on the "Single-Task and Multi-Task Modes"

portion of Intel to anticipate the throughput and wide operational modes of Claims 19 and 31. (Page 13 of the final Office action.) In that section, Intel describes how the processor may be operated in either a multi-task (MT-mode), in which both *logical* processors are employed, or single-task (ST0-more or ST1-mode), in which only a single logical processor is used. However, in either case, only a single *physical* processor, with a single set of execution units, is used no matter what mode is invoked. The purpose of the single-task modes is to recombine previously partitioned resources, such as the execution trace cache (TC) and the "uop queue," to a single logical processor. Also, as noted above, the execution units are *not* partitioned between logical processors, and thus operate in the same manner regardless of whether the operations executed are associated with one or more logical processors. Thus, Intel does not teach or suggest distributing instruction bundles to more than one cluster of execution units based on a mode of operation, as provided for in claims 19 and 31.

Further, presuming that either of the single-task modes ST0 and ST1 is employed when a single software thread is executing, then only a *single* logical processor is employed, utilizing the single physical processor available. The other logical processor is halted under that scenario by way of the HALT instruction. Thus, Intel does not even teach or suggest issuing bundles of instruction from a single thread to more than one *logical* processor, much less to more than one physical processor. Thus, Intel does not teach or suggest a wide mode of operation, as provided for in claims 19 and 31, and such indication is respectfully requested.

Thus, based on the foregoing, the Assignee contends that claims 19 and 31 are allowable in view of Intel, and such indication is respectfully requested.

Claims 20-30 depend from independent claim 19, and claims 32-34 depend from independent claim 31, thus incorporating the provisions of their corresponding independent claims. Thus, the Assignee asserts that claims 20-30 and 32-34 are allowable for at least the reasons presented above in support of claims 19 and 31, and such indication is respectfully requested.

Therefore, in light of the foregoing, the Assignee respectfully requests the withdrawal of the 35 U.S.C. § 102 rejection.

Conclusion

Based on the above remarks, the Assignee submits that claims 19-34 are allowable. Additional reasons in support of patentability exist, but such reasons are omitted in the interests of clarity and brevity. The Assignee thus respectfully requests allowance of claims 19-34.

The Assignee hereby authorizes the Office to charge Deposit Account No. 08-2025 the appropriate fee under 37 C.F.R. § 1.17(e) for the request for continued examination (37 C.F.R. § 1.114(a)). The Assignee believes no fees are due with respect to this filing. However, should the Office determine additional fees are necessary, the Office is hereby authorized to charge Deposit Account No. 08-2025.

Respectfully submitted,

Date: 1/31/07

SIGNATURE OF PRACTITIONER
Kyle J. Way, Reg. No. 45,549
Setter Roche LLP
Telephone: (720) 562-2283
E-mail: kyle@setterroche.com

Correspondence address:

CUSTOMER NO. 022879

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400